BACKDRIVING: The Force Behind Functional Test

In order to test functionality of a digital integrated circuit without removing it from a Panel electronic Circuit (PEC), the inputs of the IC must be driven to both high and low states according to a pre-determined test pattern. Since these inputs will usually be driven by other IC's on the PEC, it is necessary to temporarily over-ride or back drive these other outputs in order to force the required levels onto the inputs of the IC under test. The usual way in which this is done is by the use of high current drives that can sink or source more current than the outputs being back driven.

The worst case condition, for the TTL IC's, is when low output needs to be pulled up to a high level, since the sink current capability of a TTL output is much higher than it's source current capability. Most TTL outputs have a resistor in the upper "leg" of the output stage, which effectively limits the current required to pull down a high output in a low state.

It is apparent that the currents that flow in these circumstances will be higher than normal operating currents, and therefore consideration has to be given to the likelihood of damage being caused to the backdriven IC. Damage may be caused directly to the junction by over dissipation occurring, or to the bond wire by excessive heating due to large current flow. A further mechanism which could cause bond wire damage, related to temperature cycling, is identified in DEF STAN 00-53/1

Many different manufacturers produce In-Circuit A T E systems that use the backdriving technique to perform functional test of IC's. They are usually used on PEC's as part of the production test process. This means that any stresses that result from backdriving are applied to each and every PEC, regardless of its functional state. The **Boardmaster 8000 PLUS** and **SYSTEM 8** products are only used on PEC's that are known to be faulty and that have already stresses in some way during operation. There are many risks involved in the process of the board repair, including static damage, soldering thermal damage, voltage spikes, probing shorts and PEC mechanical damage. The probability of damage caused to a PEC under repair by backdriving stress during the repair process is statistically much less than damage by other mechanisms listed above, provided the backdriving parameters are held within safe limits.

Several studies have been carried out to try to quantify the effects of backdriving on both short and long term reliability of digital IC's. All conclude that no detrimental effects can be shown to have taken place as a result of backdriving, provided that the backdriving parameters, particularly the output currents are limited to sensible values. Furthermore ABI have over 5000 backdriving systems installed world wide using the similar design of output stages, and no complaints of whether short or long term damage have been received. The system in use by the armed forces all around the world as well as hundreds of well known international organisations, each with varying

applications, has proven that the **Boardmaster 8000 PLUS** and **SYSTEM 8** provide a safe and valuable technique in in-circuit testing.

Output stage characteristics

The voltage against current relationship for both high to low and low to high backdriving for the **Boardmaster 8000 PLUS** and **SYSTEM 8** does not force any particular voltage. Systems trying to achieve a given voltage could result in current flow far greater that required. The high forcing voltage is about 3.7 volts for no load, but is maintained above TTL Minimum of 2.0 volts for the source currents up to 350mA. The low forcing voltage is maintained below 0.8 volts for sink currents up to about 170mA.

It may be concluded that backdrive currents of 500mA low to high and 200mA high to low are required in all cases. This would give vastly inflated idea of the actual current flow encounted in a typical case. The output stage is designed to only supply enough current to apply a valid logic level, low or high, so that in all but a few cases the currents measures with the system are substantially less than the maximums available. They are also in most cases much less than the values given in DEF Stan 00-53/1.

It can be seen that in many cases the actual current flow is much less than that assumed in the standard. This means that the backdriving currents used in the calculation of bond wire temperature rise will be substantially less, leading to longer allowable pulse widths up to DC steady state conditions in most cases. A further margin of safety is obtained with the **Boardmaster 8000 PLUS** and **SYSTEM 8** by relaxing the input voltage requirements of the IC under test, which are normally required to give adequate noise immunity in a functioning circuit. During a test of a single IC this requirement is not critical because the operation of the rest of the PEC is of no significance and it is only necessary that the input levels are not hovering around the threshold voltage. The currents required, with some logic families, to achieve normal operating values of input low and high voltages would be too great to carry out safely.

The signals applied in the inputs of the IC under test are generated “on the fly” by directly manipulating output ports connected to the output driver stages. As such it is impossible to give a global measure of pulse widths, as would be the case with a system which clocked the test pattern out of memory at a fixed rate. The pulse widths can only be accurately specified for a particular IC with particular circuit coditions.