

Functional IC Test Generating Software for Compact Professional Range

- Library development manager for IC configuration
- PLIP language for full generation of new IC functional tests
- Compiler, debugger and active help integrated
- Connection to PC via RS-232 or USB (with adapter)

| | | PromierLink IC Test Debugger – uA741 |
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| LineerMenter Compact | ChipManter Company | Pier Edit: Debug Tools Help Tel III III III III III IIII IIII IIII I |
| | A CONTRACTOR OF | Source Programme for uA741 |
| Putational abi | | PROCEDURE FS_TEST_AND "Neasure the nominal circuit voltage on the Will |
| 2 | 22 0 | VHCH = VOLTACE (HINV_FIN) *check we can drive the non investing around th "default to test fails |
| | | PB_TEST_PASS = 0 *first try test with nominal circuit conditions *fit they are below +/-57 |
| | | <pre>IF ADS(VNOM) < 9 *but make sure power supplies are not exceent *but make sure power supplies are supplies are not exceent *but make supplies are not supplies are not exceent *but make supplies are not supplies are not exceent *but make supplies are not s</pre> |
| | | VTEST_HIGH = VNOM + 0.14 IF VTEST_HIGH > VPLUS VTEST_HIGH = VNOM |
| | | END IF VTEST_LOW = VDOM - 0.14 |
| 00000 | 00000 | EF VTEST_LOW < VMINUS WTEST_LOW = VNOM END IF |
| 60600 | 00000 | DO FEEDACICTEST END IF |
| | | <pre>If FB_TEST_FASS = 0 *test failed, next try test around centre o *test failed, next try test around centre o </pre> |
| | | Lan 111 Chandra 2126 |

| | Name Copy of 74100 Fund | | | | | |
|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|-------------------------------|--------|---------|--------|---------|
| PromierLink IC Test Dehugger - uA741 | Device Womekon BFL Test AICT Test DipMa | oter Text LineatMaster Text | | | | |
| Edit Debug Tools Help | Device Info | Pin Out | | | | |
| | Package CIL | Number of pins 24 | - | | | |
| 📲 👪 🗈 🕴 🕈 No debug hardware 💌 🕮 🕪 🗵 📰 🖉 | | Pin No Pin Name | VCC+ I | END VCC | High V | |
| wice Programme for uA741 | Class Letch • | 1 NC | | | | · More |
| | and a second | 2 101 | | | | Hinn |
| ROCEDURE PE TEST AND | TriState Low Threshold 0.9/ | 3 102 | | | | Stowy |
| Measure the nominal circuit voltage on the NINV pin | Open Collector Switch Theehold 12V | 4 102 | | | | |
| NOM = VOLTAGE (NENV_FIN) | OpenEniter HighThreshold 2.4/ | 5 101 | | | | |
| check we can drive the non inverting around the nominal voltage | Index Copy of 74100 Tech | 6 NC | | | | Add |
| default to test fails | Vanion 2.62 | 7 GND | | | | |
| B_TEST_PASS = 0 | Date 28/07/2006 | 8 201 | | | | - Dette |
| first try test with nominal circuit conditions if they are below +/-97 | VPSAT - | E8.98 | | | | |
| 7 ADB (VBOR) < 9 | VNCM | | | | | |
| "but make sure power supplies are not exceeded | VPCM | EBAD | | | | |
| VTEST HIGH * VNOM + 0,14 | MAR_OUTPUT_VOLTAGE | EBA2 | | | | |
| IF VIEST_HICH > VPLOS | COMP_TEST_PASS - FRRATIO - | EBAB | _ | | | |
| WTEST_HIGH + VHON | FD_TEST_PASS - | EBAP | | | | |
| END IF | VPLUS - | | | | | |
| VTEST_LOW = YNON - 0.14 | VMINUS - | | | | | |
| IF VIEST_LOW < VMIMUS | VTEST - | E88F | | | | |
| VTEST_LOW = VNOM | VIN | | | | | |
| END 17 DO FEEDBACICTEST | VCENTRE - | E8C7 | | | | |
| DU FELIGALKIESI SD 17 | OP_PIN - | EBCB | | | | |
| Y PE TEST PASS = 0 | | 7817 | _ | | | |
| *test failed, next try test around centre of supplies | Result | | | | | |
| 10000 1000 10000 10 10 | Beaut | | | | | |
| ne 111 Duracter 328 | IC pin status | Display output | | | | |
| A | Pin None Foult Fe | | | 140 | | |
| | 1 0/14 | | | 1 | | |
| luid Statut Build Eases Warrings Info | 2 INV | | | | | |
| Trip Noncortlin setting | 3 NNV | | | | | |
| inces Trip-No list lie specied | 4 V. | | | | | |
| Info - No object file specified | 5 0/NU. 6 0UTP. | | | | | |
| Varnings Time Info - Compiler started at 13:38:21 on 10 August 2006 | 7 04 | | | | | |
| Into - PLIP exurce lie detected Into - Define parameter MAX, OFFSET', 4 bates | 8 NC | | | | | |
| Info - Define parameter 1POS ¹ 4 bates | 24 - 24(T) | | | | | |
| Info - Define parameter INEG', 4 bytes | | | | | | |
| Info - Define parameter VMSAT', 4 bates | | | | 1 | | |
| Info - Deline parameter VPSAT', 4 bytes | c 3 | | | 1 | | |
| Into - Define parameter VMDM, 4 butes | | | | | | |

CompactLink Software

A PC based software package that allows users to add new devices to the library and create functional tests to suit special applications.

New IC functional tests can be created using *PremierLink IC Programming* (PLIP), a high-level descriptive test programming language optimised for generation of both analogue and digital IC test programmes.

Thanks to the RS-232 link, software updates (available on the internet) can be downloaded and programmed into the Compact units. This active link also allows for live testing of new devices.





CompactLink Software

Library Development Manager

The Library Development Manager displays all the devices added to the library and saved in the USER family.

All details are stored in the Microsoft AccessTM compatible database file located in the PremierLink folder.

The device data is organised in 20 families and can be filtered using the drop down menus. A device name or function can also be typed in to facilitate the search. The list will be filtered to show only the entries containing the entered text. As an option, *intelligent sort* produces a more logical list by using the numeric part of the device name only.

| Name Copy of 74100 Fu | nction 8 BIT BIS | TABLE LATCH | | | | Family US | ER 👱 |
|---------------------------------------------|--------------------|----------------|------|-----|------|-----------|--------------|
| Device Information BFL Test AICT Test Chipt | daster Test Line | sarMaster Test | | | | | |
| Device Info Package DIL | Pin Out Numbr | erofpins: 24 | | | | | |
| | Pin No | Pin Name | VCC+ | GND | VCC- | High V | |
| - | 1 | NC | | | | | Move |
| Class Latch 💌 | 2 | 1D1 | | | | | Up |
| Tri State Low Threshold 0.5V | 3 | 1D2 | | | | | Move Down |
| Open Collector Switch Threshold 1.2V | 4 | 102 | | | | | |
| Open Emitter High Threshold 2.4 | 5 | 101 | | | | | |
| Index Copy of 74100 Tech | 6 | NC | | | | | Add |
| Version 2.62 | 7 | GND | | | | | |
| Date 28/07/2006 | 8 | 201 | | | | | Delete |

Programming Interface

The Programming Interface is designed for the generation and debugging of new functional IC tests. PLIP (PremierLink IC Programming) is a high level language designed specifically for test programming. The syntax is highly descriptive so that programmes are, to a large extent, self commenting. However, comments can also be inserted if required.

The built in compiler generates binary data which can be executed in stand alone form by the integral debugger or combined into library files for use with System8 products. Up to 3 breakpoints can be added to the programme where execution can be suspended and data can be examined. The debugger allows the user to identify and fix the possible problems in the programme, whilst connected to the hardware, before adding the new device to the library.

Device Definition

When a device is selected or created, the device definition window appears. This allows the user to enter the information related to the device as well as define its physical characteristics. The name and function will be used by the database for sorting. Parameters such as package, class, thresholds and output types may also be selected.

The power and ground pins of the new device must be specified using the pin out table.





Online Active Help

CompactLink is supplied with an extensive online active help which can be accessed at any time during programming. This facility provides the user with a PLIP syntax guide for each command. The Active Help window is broken down into :

- A syntax section
- An extensive description of the command
- Concrete examples for illustration
- Additional comments (if applicable)
- Target field



Making Light Work

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